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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	6	Attorney Docket Number
				TSM03-0698

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
KJ	1	US-4,069,094	01-17-1978	Shaw et al.	
	2	US-4,314,269	02-02-1982	Fujiki	
	3	US-4,497,683	02-05-1985	Celler et al.	
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Examiner Signature	Keith Quarto	Date Considered
		6/28/05

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Sheet	2	of	6	Attorney Docket Number	TSM03-0698
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Complete if Known

Application Number	10/786,643
Filing Date	2/25/2004
First Named Inventor	Cheng, et al.
Art Unit	2826
Examiner Name	Quinto, Kevin

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (U.S. only)			
KL	40	US-2002/0125471 A1	09-12-2002	Fitzgerald et al.	
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	75	US-6,803,641 B2	10-12-2004	Papa Rao et al.	

Examiner Signature	Keith Duhrt	Date Considered	11/20/05
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<p>Substitute for form 1449A/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p><i>(Use as many sheets as necessary)</i></p>				<p>Complete If Known</p> <table border="1"> <tr> <td>Application Number</td> <td>10/786,643</td> </tr> <tr> <td>Filing Date</td> <td>2/25/2004</td> </tr> <tr> <td>First Named Inventor</td> <td>Cheng, et al.</td> </tr> <tr> <td>Art Unit</td> <td>2826</td> </tr> <tr> <td>Examiner Name</td> <td>Quinto, Kevin</td> </tr> <tr> <td>Attorney Docket Number</td> <td>TSM03-0698</td> </tr> </table>		Application Number	10/786,643	Filing Date	2/25/2004	First Named Inventor	Cheng, et al.	Art Unit	2826	Examiner Name	Quinto, Kevin	Attorney Docket Number	TSM03-0698
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FOREIGN PATENT DOCUMENTS

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		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)			
MM	76	EP 0 683 522 A2	11-22-1995	International Business Machines Corporation	
MM	77	EP 0 828 296 A2	03-11-1998	International Business Machines Corporation	
MM	78	WO 03/017336 A2	02-27-2003	Amberwave Systems Corporation	

NON-PATENT LITERATURE DOCUMENTS

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	79	"Future Gate Stack," International Sematech, 2001 Annual Report.		
	80	"BEDNAR, T.R., et al. "Issues and Strategies for the Physical Design of System-On-A-Chip ASICs," IBM J. RES. & DEV., Vol. 46, No. 6 (November 2002) pp. 661-674.		
	81	BLAAUW, D., "Gate Oxide and Subthreshold Leakage Characterization, Analysis and Optimization," date unknown.		
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Examiner Signature	Keith Quinto	Date Considered	6/20/05
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<i>QZ</i>	83	CHANG, L., et al., "Direct-Tunneling Gate Leakage Current in Double-Gate and Ultrathin Body MOSFETs," 2002 IEEE Transactions on Electron Devices, Vol. 49, No. 12, December 2002, pp. 2288-2295.			
<i>QZ</i>	84	CHANG, L., et al., "Reduction of Direct-Tunneling Gate Leakage Current in Double-Gate and Ultra-Thin Body MOSFETs," IEEE, 2001, 4 pages.			
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Examiner Signature	<i>Kevin Quinto</i>	Date Considered	4/20/05
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Sheet	5	of	6	Attorney Docket Number	TSM03-0698

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<i>K2</i>	94	LEITZ, C.W., et al., "Hole Mobility Enhancements In Strained Si/Si _{1-x} Ge _x P-Type Metal-Oxide-Semiconductor Field-Effect Transistors Grown On Relaxed Si _{1-x} Ge _x (x<y) Virtual Substrates," Applied Physics Letters, Vol. 79, No. 25, December 17, 2001, pp. 4246-4248.				
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Examiner Signature	<i>Kevin Quinto</i>	Date Considered	<i>11/20/05</i>
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	106	SHIMIZU, A., et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," IEDM 2001, pp. 433-436.		
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	108	THOMPSON, S., et al., "A 90 nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 um ² SRAM Cell," IEDM, December 2002, pp. 61-64.		
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<i>QJ</i>	115	YEOH, J.C., et al., "MOS Gated Si:SiGe Quantum Wells Formed by Anodic Oxidation," Semicond. Sci. Technol., Vol. 13, 1998, pp. 1442-1445.		

Examiner Signature	<i>Kevin Quinto</i>	Date Considered	1/20/03
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